## DDCO Assignment

## Week 1

## Basic Gates, Universal Gates, XOR, XNOR Gates and Full Adder

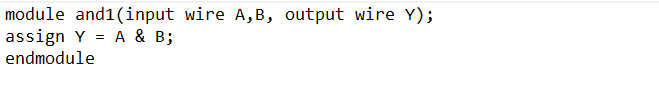
Name : Renita Kurian

SRN : PES1UG20CS331

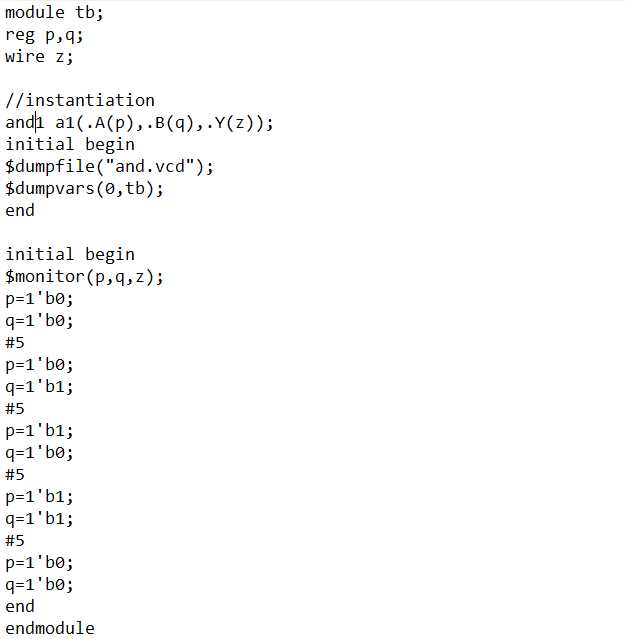
Roll No. : 27

Section : F

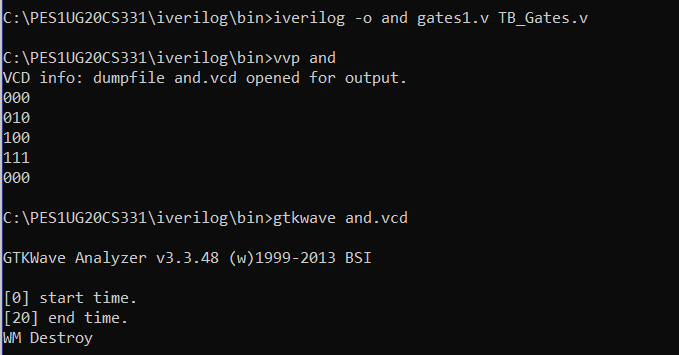
1. AND Gate

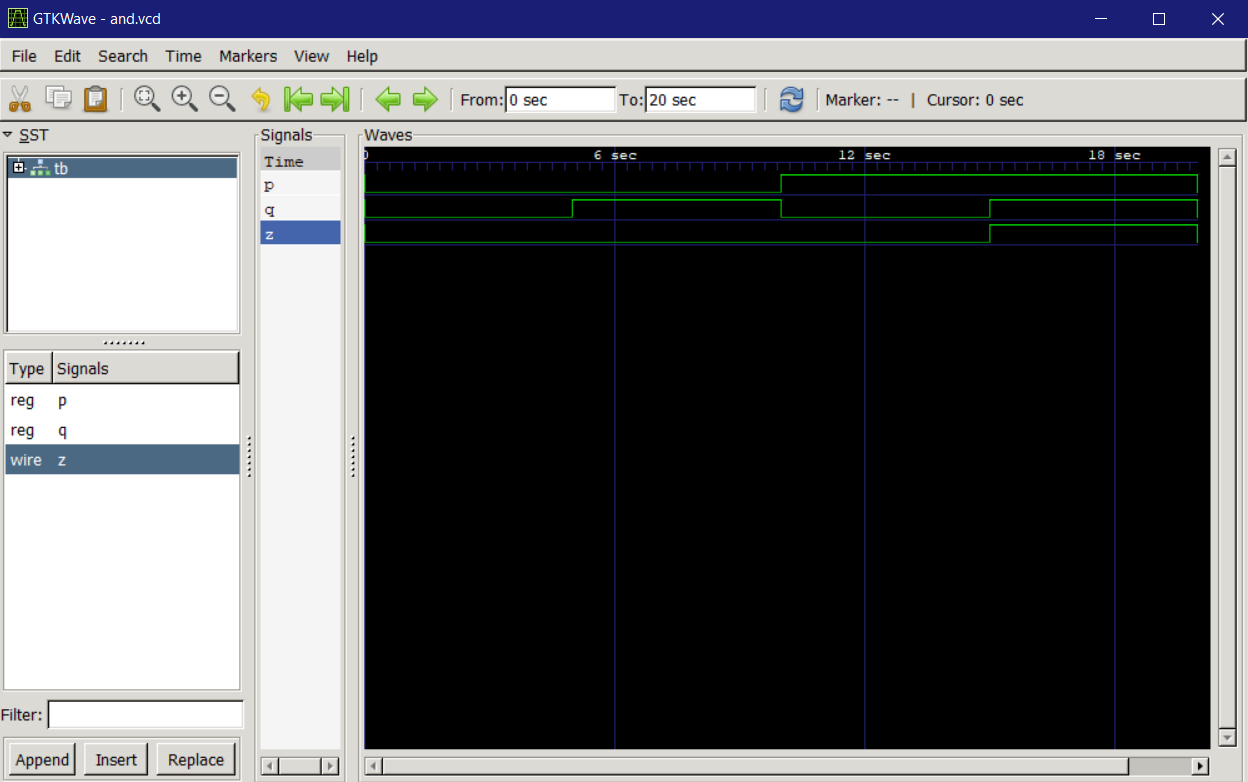


Testbench file –

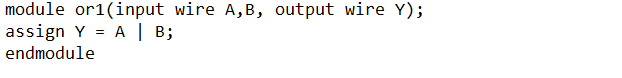


Output –

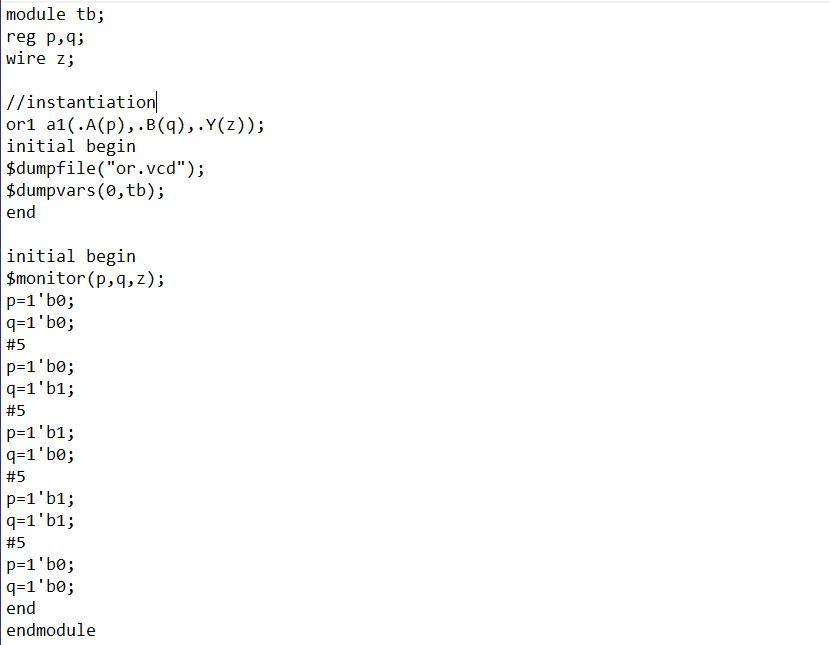




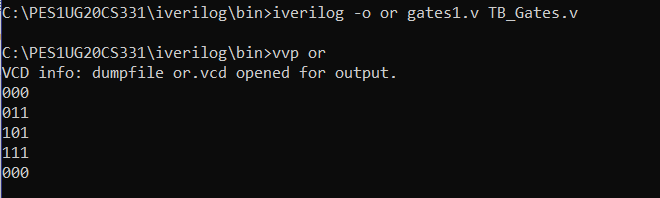
1. OR Gate

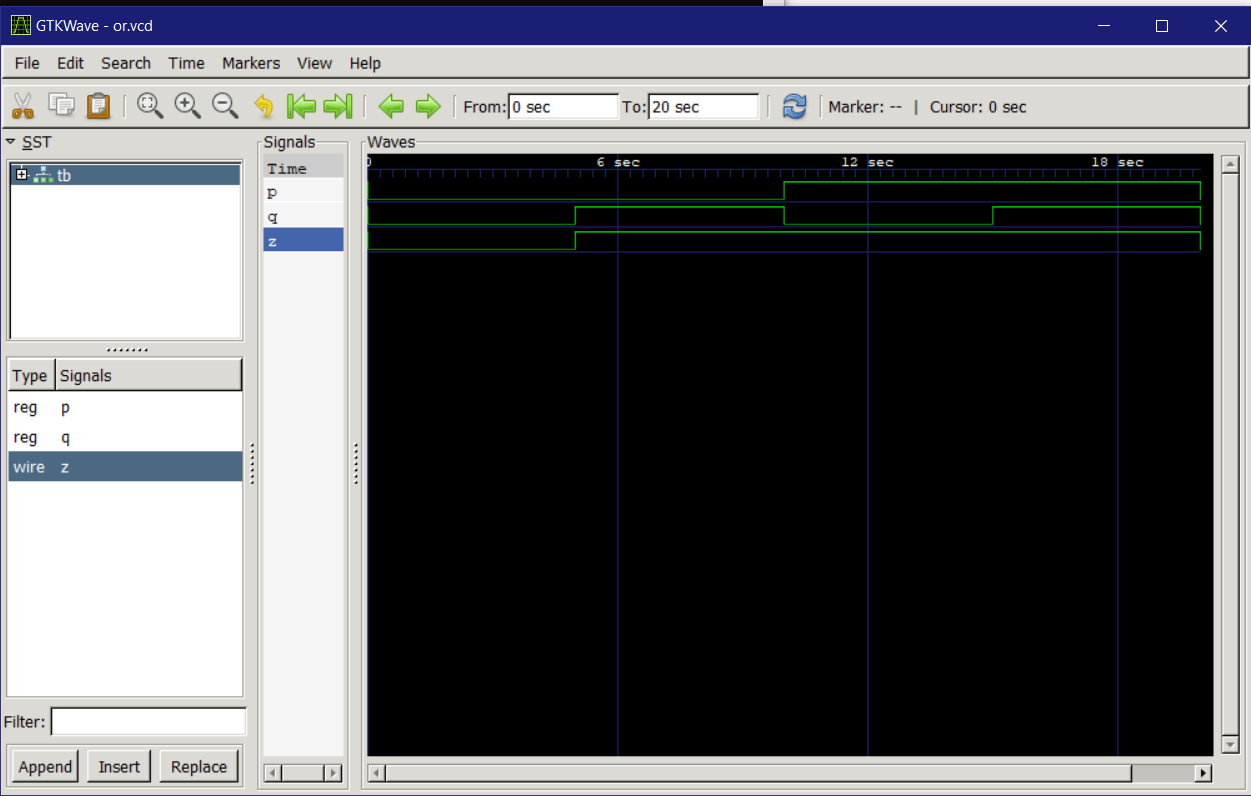


Testbench file –

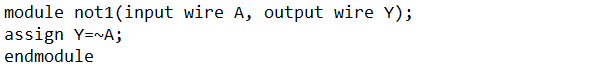


Output –

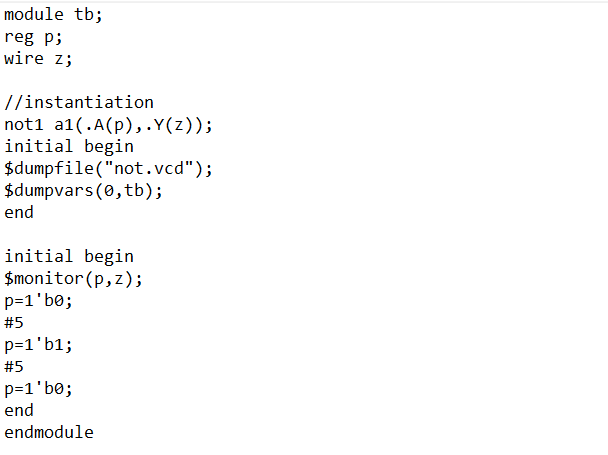




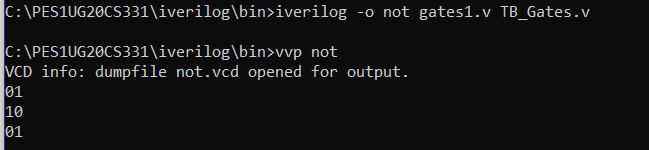
1. NOT Gate

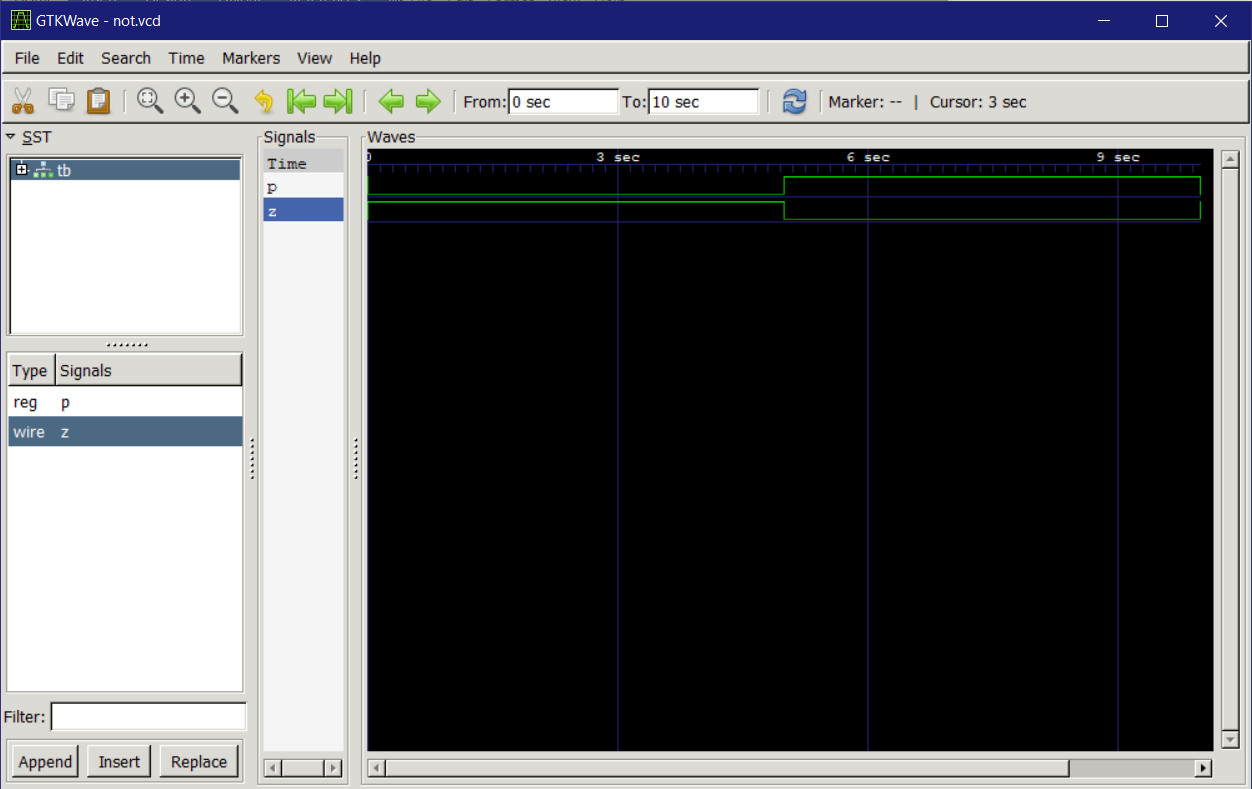


Testbench file –

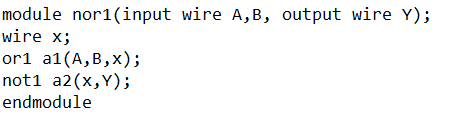


Output –

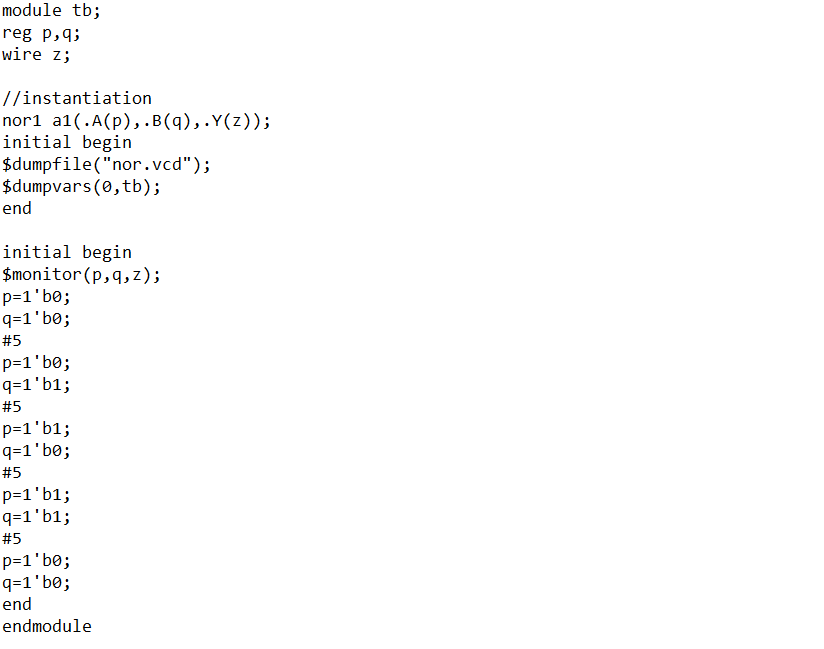




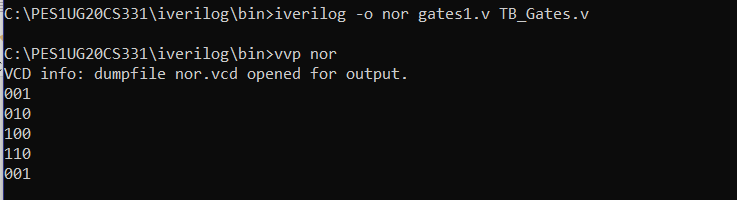
1. NOR Gate

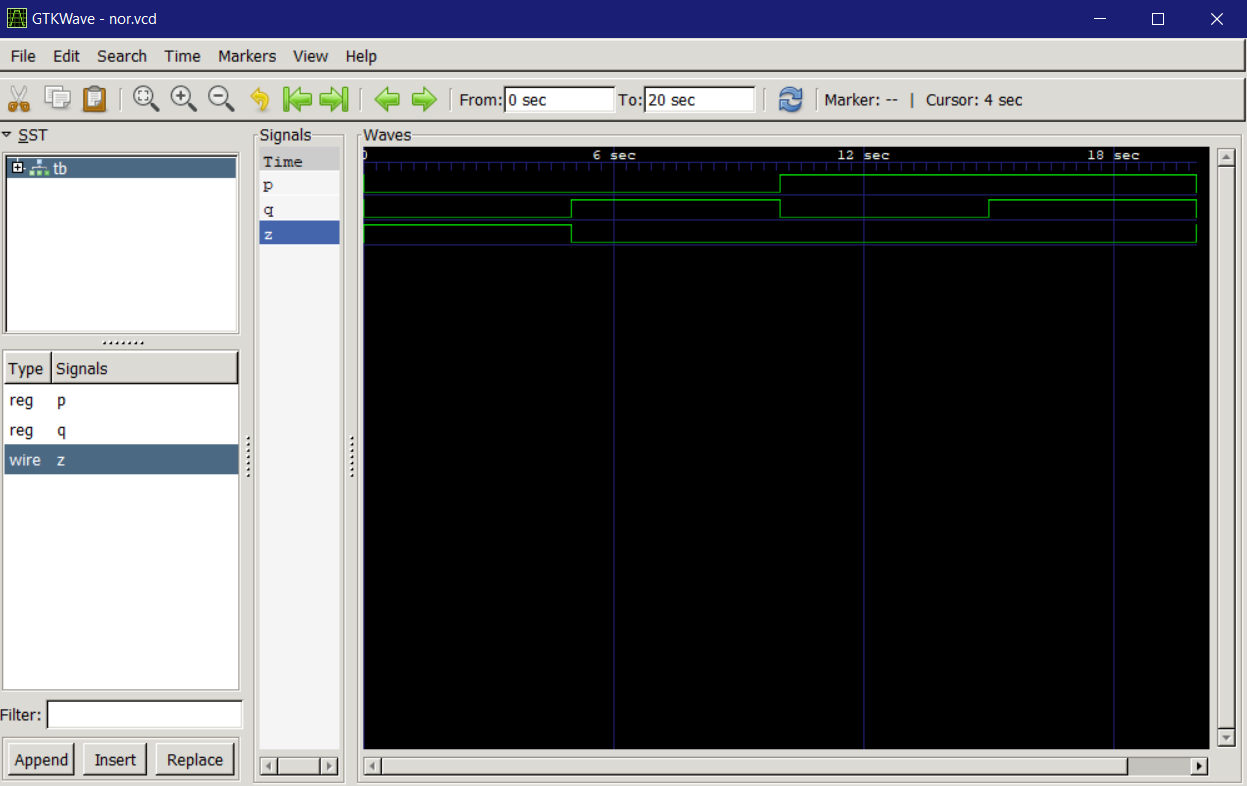


Testbench file –

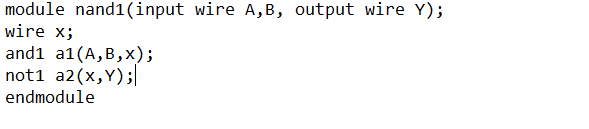


Output –

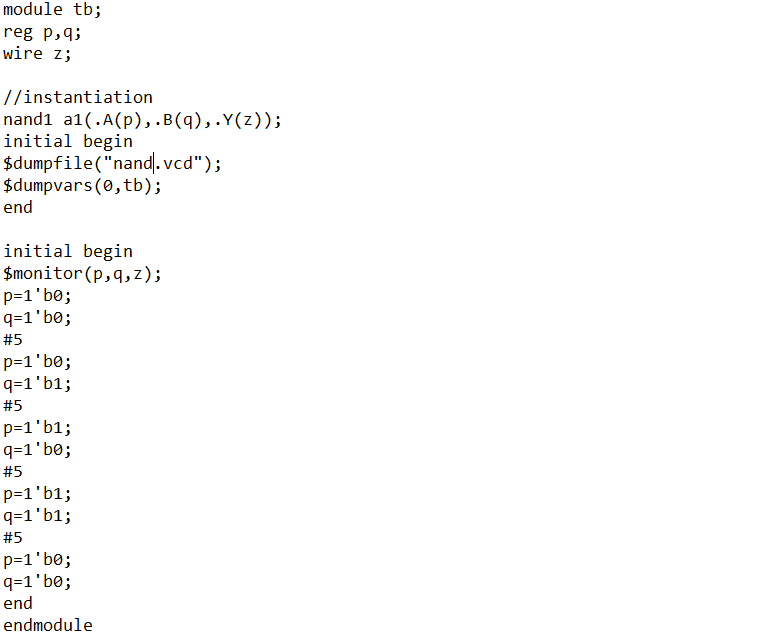




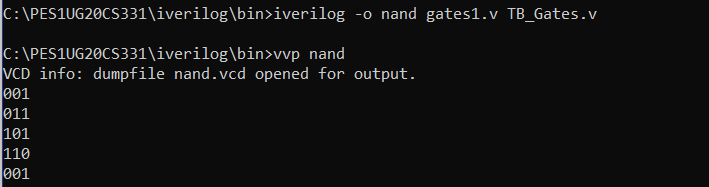
1. NAND Gate

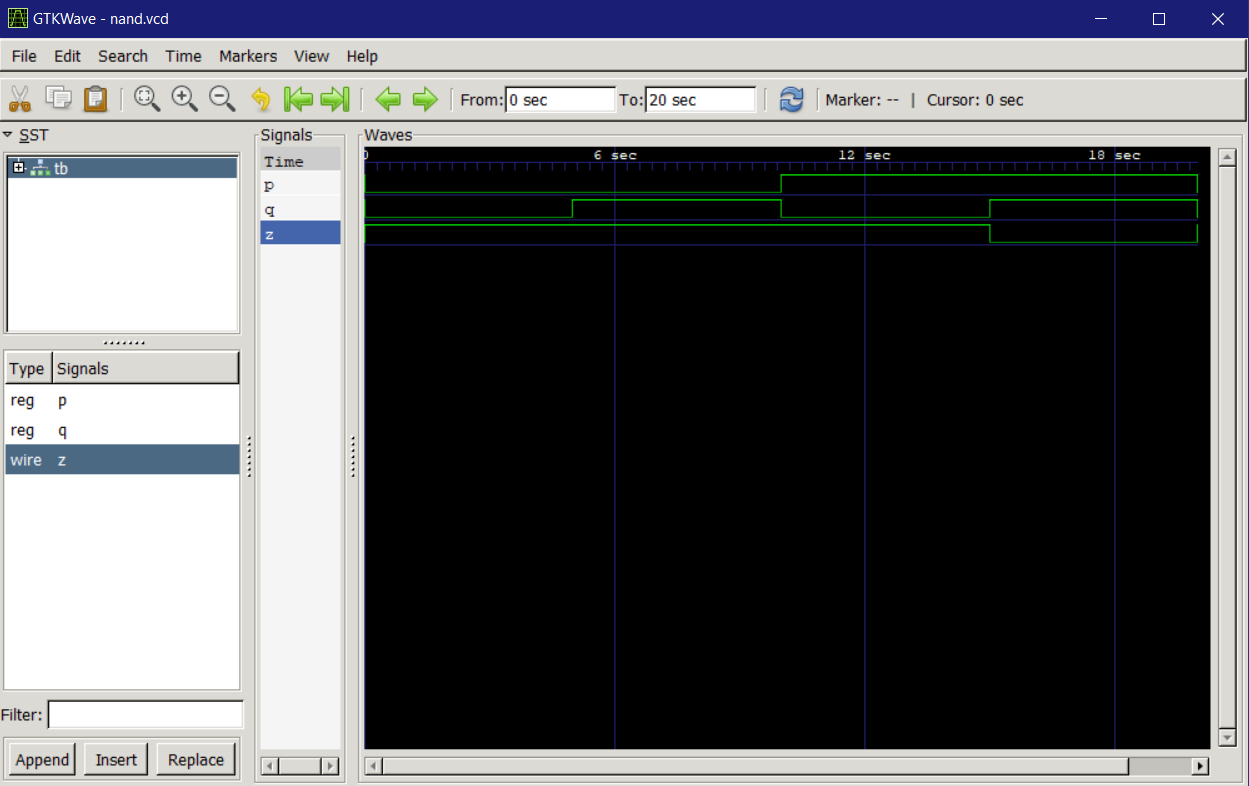


Testbench file –

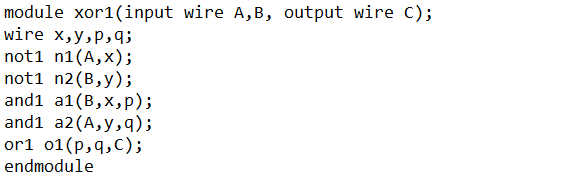


Output –

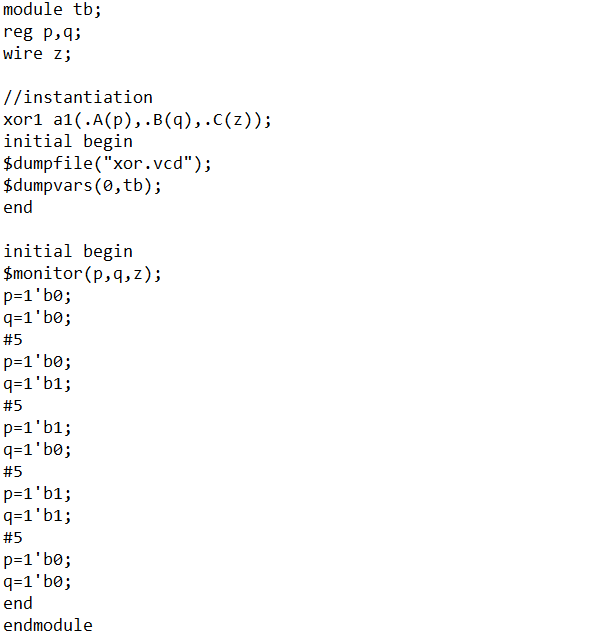




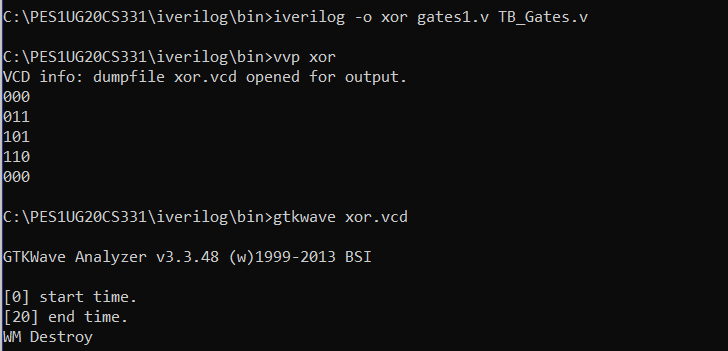
1. XOR Gate

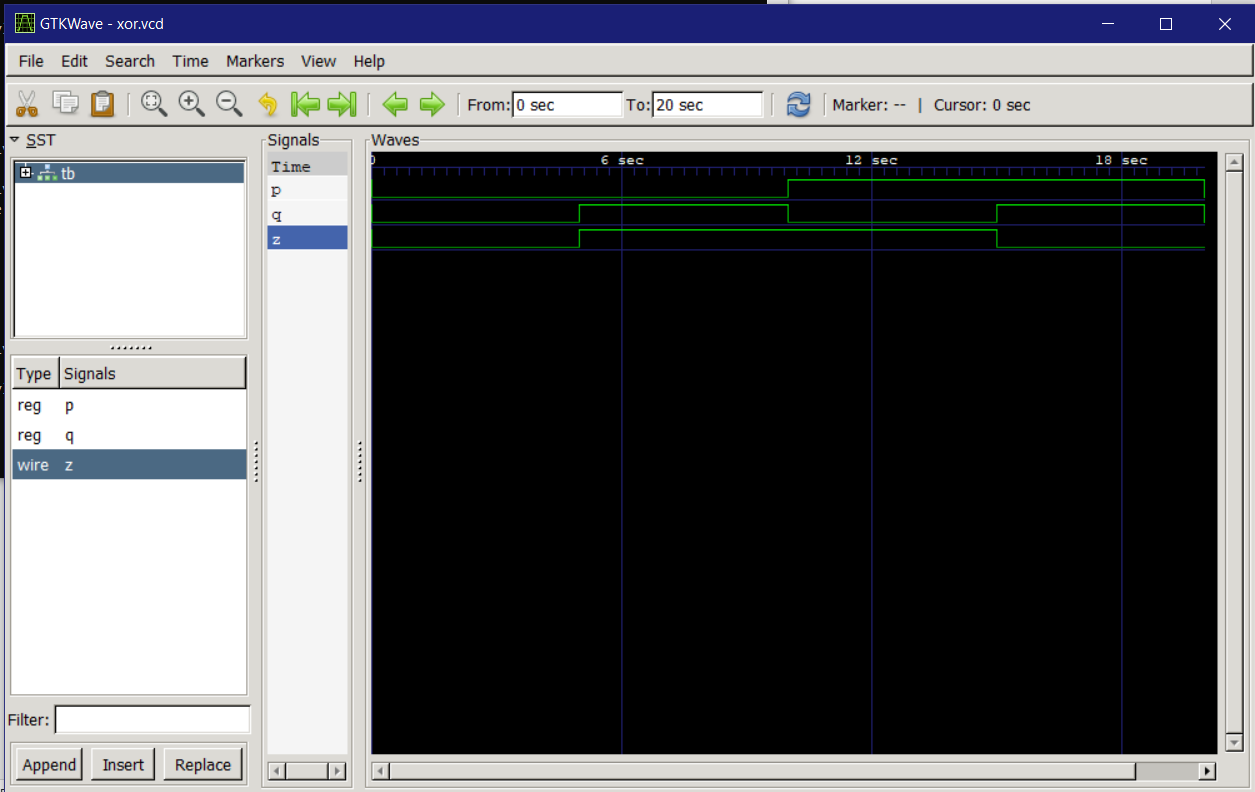


Testbench file –

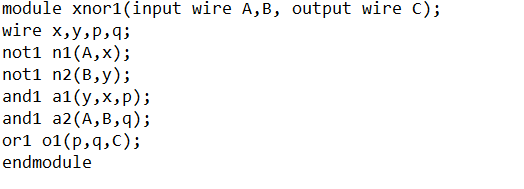


Output –

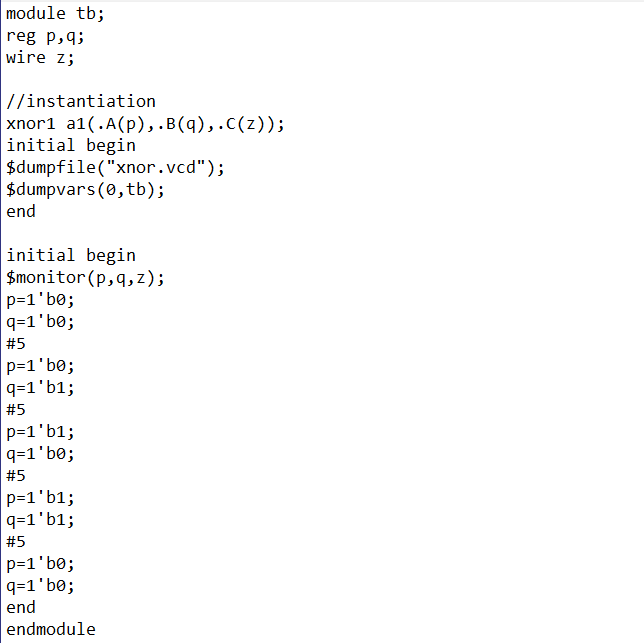




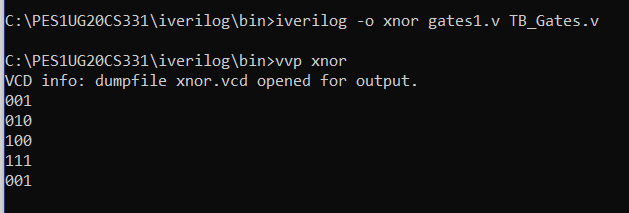
1. XNOR Gate

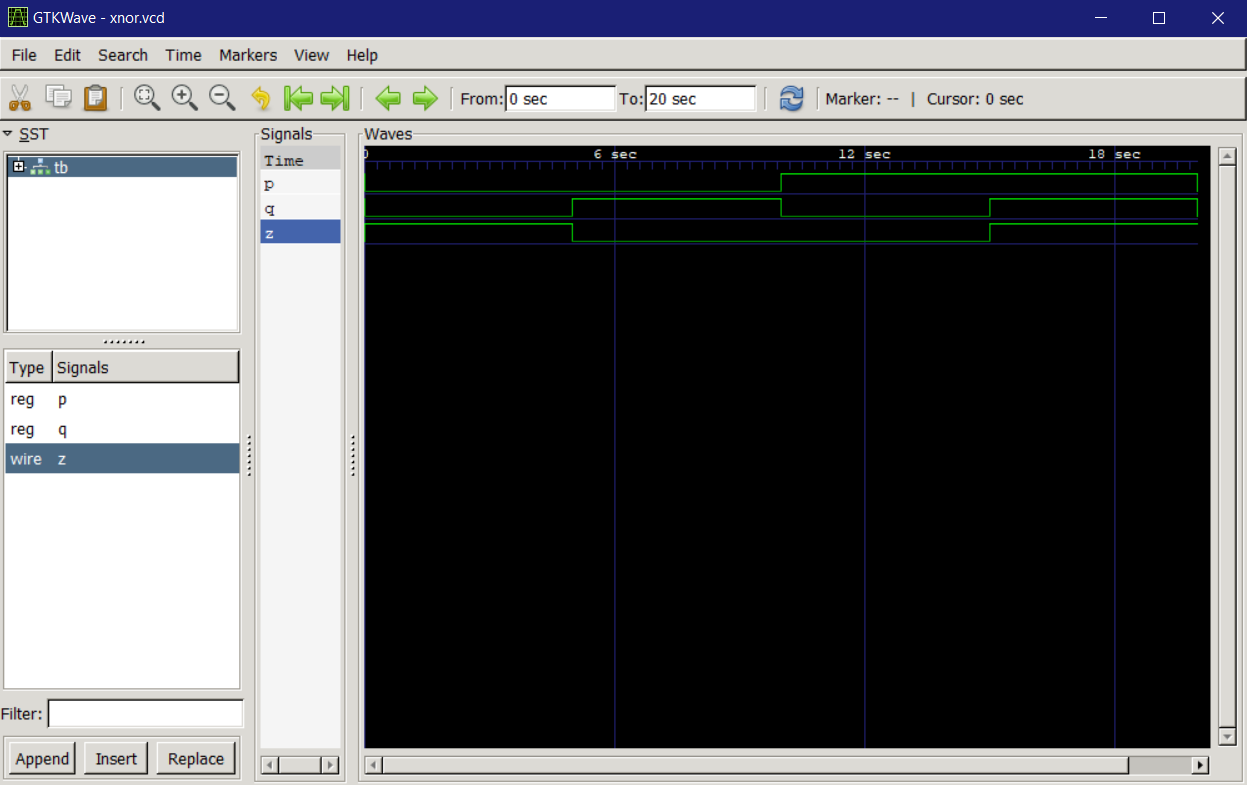


Testbench file –

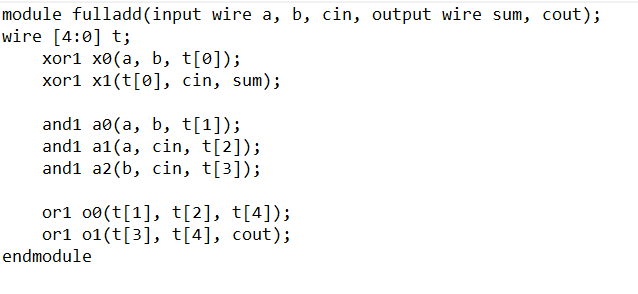


Output –

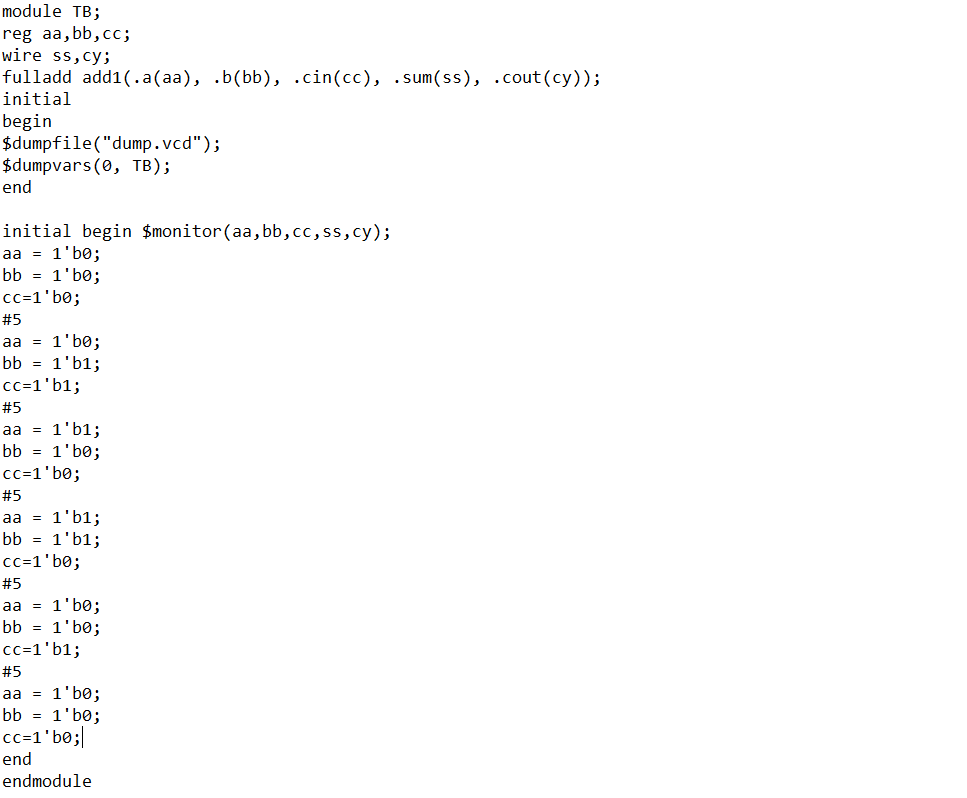




1. Full Adder



Testbench file –



Output –



